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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,366	11/19/2003	Tetsuya Yoshida	1448.1047	3769
21171	7590	01/13/2006	EXAMINER	
STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			KO, DANIEL BOKMIN	
			ART UNIT	PAPER NUMBER
			2189	

DATE MAILED: 01/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/715,366	<b>Applicant(s)</b> YOSHIDA ET AL.	
	<b>Examiner</b> Daniel B. Ko	<b>Art Unit</b> 2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 19 November 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 3, 5-8, 10-13 is/are rejected.
- 7) ☒ Claim(s) 2, 4 and 9 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>11/19/2003</u> . | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

This action is responsive to the application filed on 11/19/2003. Claims 1-13 have been submitted for examination.

#### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 7 recites the limitation "the nonvolatile" in 2<sup>nd</sup> line of the claim. There is insufficient antecedent basis for this limitation in the claim.

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1, 3, 5-8, 10-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Cleveland et al. (US Patent 6,285,583 B1), hereinafter simply Cleveland.

Regarding claims 1, 3, and 8, Cleveland teaches a memory control circuit comprising a write error protect circuit that disables output of a write signal supplied from outside to a memory by resetting a register (column 12, lines 13-60), outputs the

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write signal supplied from the outside to the memory upon writing a first data into the register (column 12, lines 32-34; Cleveland discloses the unlock signal), and prevents the output of the write signal to the memory upon writing a second data that is different from the first data into the register (column 12, lines 32-34; column 13, lines 7-24; Cleveland discloses the lock signal and the sector enable latch signal).

Regarding claims 5 and 10, Cleveland teaches a memory device, wherein the memory is divided into a plurality of areas in which write disable, write enable, and write error protect are set independently; and the memory includes the write error protect circuit for each area (See Fig. 2, column 11, lines 21-43).

Regarding claims 6 and 11, Cleveland teaches a memory device, wherein the memory is a nonvolatile memory (column 4, lines 62-67; Cleveland discloses a flash memory device which is a type of nonvolatile memory).

Regarding claims 7 and 12, Cleveland teaches a memory device, wherein the nonvolatile memory is a flash memory (column 4, lines 62-67).

Regarding claim 13, Cleveland teaches a microcomputer, wherein the central processing unit, the memory, and the memory control circuit are integrated in a same semiconductor chip (column 5, lines 48-56).

***Allowable Subject Matter***

2. Claims 2, 4, and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: With respect to claims 2, 4, and 9, the prior art fails to teach a specific write error protected circuit includes a first latch circuit that stores "0" by reset; a second latch circuit that stores "1" by reset, to which an output signal from the first latch circuit is input; a first gate that outputs a register setting data supplied from the outside to the first latch circuit when an output signal from the second latch circuit is "1", and outputs "0" to the first latch circuit when the output signal from the second latch circuit is "0"; and a second gate that outputs a write signal supplied from the outside to the memory only when the output signal from the first latch circuit is "1".

**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel B. Ko whose telephone number is 571-272-8194.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Manorama Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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AU 2189



**MANO PADMANABHAN**  
**SUPERVISORY PATENT EXAMINER**